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EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/802,857	Applicant(s) KOH ET AL.	
	Examiner Michael J. Yigdall	Art Unit 2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 are pending and have been examined. The priority date considered for the application is 14 March 2000.

Drawings

2. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Figures 1 and 2 are described under the heading "Description of the Related Art," and are shown to illustrate an example of a conventional data processing apparatus, rather than an embodiment of the present invention (see page 14).

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Pat. No. 5,454,100 to Sagane.

With respect to claim 1, Sagane discloses a data processing apparatus performing predetermined data processing in accordance with instruction codes read from a memory storing a program (see column 1, lines 9-14), comprising:

(a) an address holding means for holding a bug address showing the start of a buggy part of the program stored in the memory (see EEPROM 13 in FIG. 1 and column 3, lines 32-34, which shows holding the starting address of a program portion to be corrected),

(b) a comparison means for comparing a program address for reading the program from the memory with the bug address held in the address holding means during the data processing and outputting a coincidence signal when the addresses coincide (see comparator 8 in FIG. 1 and column 3, lines 48-52, which shows outputting a coincidence signal when the program address and the correction or bug address are the same), and

(c) a program executing means for performing predetermined data processing in accordance with instruction codes read from the memory when said coincidence signal is not output by said comparison means (see CPU 2 in FIG. 3 and column 6, lines 37-40, which shows reading instructions from ROM when there is no coincidence signal) and for suspending an instruction being executed, reading instruction codes from a program address designated by a predetermined address table, and performing processing according to the read instruction codes when said coincidence signal is output by said comparison means (see column 6, lines 41-52, which shows suspending normal execution and instead processing the program read from RAM, at the address designated by a table, when there is a coincidence signal).

With respect to claim 2, Sagane further discloses the limitation wherein said comparison means comprises an interrupt request means for outputting an interrupt request signal as said coincidence signal when a program address coincides with the bug address held in the address holding means (see interrupt control circuit 7d in FIG. 1 and column 5, lines 13-16, which shows generating an interrupt from the coincidence signal when the program address and the correction or bug address are the same).

With respect to claim 3, Sagane further discloses:

(a) a rewritable memory for storing a debugging program input from the outside during initialization (see RAM 4 in FIG. 1 and column 3, lines 40-46, which shows writing a correction or debugging program input from an external EEPROM to RAM during initial program loading).

(b) an interrupt vector for storing a start address of a memory area storing said debugged program (see interrupt vector register 7b in FIG. 1 and column 4, lines 16-21, which shows storing the start address of the correction or debugging program in the interrupt vector).

With respect to claim 4, Sagane further discloses the limitation wherein said program executing means comprises an interrupt processing means for suspending an instruction being executed when receiving said interrupt request signal, reading said debugging program from the address designated by said interrupt vector, and performing processing accordingly (see column 5, lines 13-21, which shows suspending execution as a result of an interrupt and then passing control to the correction or debugging program that is read from the address designated by the interrupt vector).

With respect to claim 5, Sagane further discloses the limitation wherein said interrupt processing means sets a return address for returning to the suspended program after the interrupt processing according to an address stored at the end of said debugging program after execution of said debugging program (see column 3, line 66 to column 4, line 7, which shows the interrupt handler returning control to the suspended program according to an address stored at the end of the correction or debugging program).

With respect to claim 6, Sagane discloses a data processing apparatus performing predetermined data processing in accordance with instruction codes read from a memory storing a program (see column 1, lines 9-14), comprising:

(a) a plurality of basic units (see column 6, line 67 to column 7, line 3) each including:

(i) an address holding means for holding a bug address showing the start of a buggy part of the program stored in the memory (see EEPROM 13 in FIG. 1 and column 3, lines 32-34, which shows holding the starting address of a program portion to be corrected), and

(ii) a comparison means for comparing a program address for reading the program from the memory with the bug address held in the address holding means during the data processing and outputting a coincidence signal when the addresses coincide (see comparator 8 in FIG. 1 and column 3, lines 48-52, which shows outputting a coincidence signal when the program address and the correction or bug address are the same),

(iii) the number of basic units corresponding to the number of bugs included in the program (see column 6, line 67 to column 7, line 3, which shows a plurality of components corresponding to a plurality of bugs), and

(b) a program executing means for performing predetermined data processing in accordance with instruction codes read from the memory when said coincidence signal is not output by said comparison means (see CPU 2 in FIG. 3 and column 6, lines 37-40, which shows reading instructions from ROM when there is no coincidence signal) and for suspending an instruction being executed, reading instruction codes from a program address designated by a predetermined address table, and performing processing according to the read instruction codes when said coincidence signal is output by any one of said comparison means (see column 6, lines 41-52, which shows suspending normal execution and instead processing the program read from RAM, at the address designated by a table, when there is a coincidence signal).

With respect to claim 7, Sagane further discloses the limitation wherein said comparison means comprises an interrupt request means for outputting an interrupt request signal as said coincidence signal when a program address coincides with the bug address held in the address holding means (see interrupt control circuit 7d in FIG. 1 and column 5, lines 13-16, which shows generating an interrupt from the coincidence signal when the program address and the correction or bug address are the same).

With respect to claim 8, Sagane further discloses:

(a) a writable memory for storing a debugging program input from the outside during initialization (see RAM 4 in FIG. 1 and column 3, lines 40-46, which shows writing a correction or debugging program input from an external EEPROM to RAM during initial program loading).

(b) an interrupt vector for storing the start address of a memory area storing said debugging program (see interrupt vector register 7b in FIG. 1 and column 4, lines 16-21, which shows storing the start address of the correction or debugging program in the interrupt vector).

With respect to claim 9, Sagane further discloses the limitation wherein said program executing means comprises an interrupt processing means for suspending an instruction being executed when receiving said interrupt request signal, reading said debugging program from the address designated by said interrupt vector, and performing processing accordingly (see column 5, lines 13-21, which shows suspending execution as a result of an interrupt and then passing control to the correction or debugging program that is read from the address designated by the interrupt vector).

With respect to claim 10, Sagane further discloses the limitation wherein said interrupt processing means comprises:

(a) an interruption recording means for recording the number of interruptions (see column 5, lines 49-54, which shows that if a plurality of bugs are to be corrected, the interrupt generating address and interrupt vector registers are updated after each correction to reflect the next one; note that for the registers to be updated in this manner, i.e. incremented or decremented to the next address, there is inherently an interrupt recording means for keeping track or keeping count of the number of corrections, and thus the number of interruptions, that have already occurred).

(b) a branch means for branching to a predetermined debugging program among a plurality of the debugging programs stored in the memory according to the number of interruptions recorded by the interruption times recording means (see column 5, lines 17-21,

which shows passing control to the address latched in the interrupt vector register, i.e. branching to the start address of the correction or debugging program; see also column 5, lines 49-54, which shows that there may be a plurality of correction or debugging programs).

With respect to claim 11, Sagane further discloses the limitation wherein an address to be returned to when returning to the original program when the debugging program is finished is stored at the end of each debugging program, and said interrupt processing means sets a return address for returning to the original program after the execution of any of the debugging programs according to the return address stored at the end of the debugging program (see column 3, line 66 to column 4, line 7, which shows the interrupt handler returning control to the suspended program according to an address stored at the end of the correction or debugging program; note that each program would have a return address).

6. Claims 1 and 6 are also rejected under 35 U.S.C. 102(b) as being anticipated by applicant's own admitted prior art (see pages 1-9).

With respect to claim 1, the admitted prior art discloses a data processing apparatus performing predetermined data processing in accordance with instruction codes read from a memory storing a program (see page 3, lines 8-10), comprising:

(a) an address holding means for holding a bug address showing the start of a buggy part of the program stored in the memory (see page 3, lines 15-19),

(b) a comparison means for comparing a program address for reading the program from the memory with the bug address held in the address holding means during the data processing and outputting a coincidence signal when the addresses coincide (see page 3, lines 19-24), and

(c) a program executing means for performing predetermined data processing in accordance with instruction codes read from the memory when said coincidence signal is not output by said comparison means and for suspending an instruction being executed, reading instruction codes from a program address designated by a predetermined address table, and performing processing according to the read instruction codes when said coincidence signal is output by said comparison means (see page 4, line 7 to page 5, line 5).

With respect to claim 6, the admitted prior art discloses a data processing apparatus performing predetermined data processing in accordance with instruction codes read from a memory storing a program (see page 3, lines 8-10), comprising:

(a) a plurality of basic units (see page 8, lines 20-25) each including:

(i) an address holding means for holding a bug address showing the start of a buggy part of the program stored in the memory (see page 3, lines 15-19), and

(ii) a comparison means for comparing a program address for reading the program from the memory with the bug address held in the address holding means during the data processing and outputting a coincidence signal when the addresses coincide (see page 3, lines 19-24),

(iii) the number of basic units corresponding to the number of bugs included in the program (see page 8, lines 20-25), and

(b) a program executing means for performing predetermined data processing in accordance with instruction codes read from the memory when said coincidence signal is not output by said comparison means and for suspending an instruction being executed, reading instruction codes from a program address designated by a predetermined address table, and

performing processing according to the read instruction codes when said coincidence signal is output by any one of said comparison means (see page 4, line 7 to page 5, line 5).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sagane, as applied to claim 10 above.

Sagane does not expressly disclose the limitation wherein said interruption recording means is a memory of a predetermined address in the rewritable memory storing the debugging programs and wherein the content of the memory is rewritten by said interrupt processing means.

However, Sagane does show an interruption recording means (see the explanation for part (a) of claim 10 above) along with rewritable memory for storing the correction or debugging programs (see RAM 4 in FIG. 1 and column 3, lines 40-46).

Examiner takes official notice that using rewritable memory such as RAM is well known in the art for holding data that may be updated but is not permanently stored, including, for example, counter values, pointers to memory addresses, and other program variables.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the RAM in the Sagane system for the interruption recording means, because storing and updating a counter value in rewritable memory is well known in the art.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant's attention is directed to European Patent Application Pub. No. 0 553 733 A2 (published 4 August 1993) and U.S. Pat. No. 6,128,751 to Yamamoto et al., which are both substantially similar to the invention claimed in the present application. Furthermore, U.S. Pat. Nos. 6,412,081 (Koscal et al.), 5,701,506 (Hosotani), 5,051,897 (Yamaguchi et al.) and 4,542,453 (Patrick et al.) also disclose comparable methods and systems for patching bugs in programs stored in memory.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (703) 305-0352. The examiner can normally be reached on Monday through Friday from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (703) 305-4552. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

Michael J. Yigdall
Examiner
Art Unit 2122

mjy
February 20, 2004

TUAN DAM
SUPERVISORY PATENT EXAMINER